

Domino Logic Circuits Capable of Reducing Power Consumption by Controlling Leakage

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The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing new circuit topologies for reducing power consumption in domino logic circuits.

Overview

In modern high-performance microprocessor circuits, gates made of an oxide, such as SiO₂, act as insulators. As electronic devices become increasingly miniaturized, gates are becoming smaller and may be composed of a layer as little as five-to-six atoms thick. Electrical current may leak through the tiny gates because they are less effective insulators than previous, thicker gates. Because gate leakage accounts for 30 to 40 percent of the total power consumption in these circuits, controlling leakage could result in huge power savings.

The Invention

UW-Madison researchers have developed new circuit topologies for simultaneously reducing the subthreshold and gate oxide leakage power consumption in domino logic circuits. Sleep transistors and dual threshold voltage complementary metal oxide semiconductor (CMOS) technology are used to place idle domino logic circuits into a low leakage state. Sleep transistors added to the dynamic nodes reduce the subthreshold leakage current by turning off at least some of the high threshold voltage transistors. Sleep switches are added to the output nodes to suppress the voltages across the gate, thus insulating layers of the transistors in the fan-out gates and minimizing the gate tunneling current.

Applications

High-speed microprocessor circuits

Key Benefits

- · Significantly decreases power consumption due to leakage at high and low die temperatures
- Because the new circuits have low speed, area and energy overhead, the subthreshold and gate oxide leakage currents are reduced.
- · Provides net savings in total power consumption during short idle periods

Tech Fields

Information Technology : Hardware

For current licensing status, please contact Emily Bauer at emily@warf.org or 608-960-9842

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