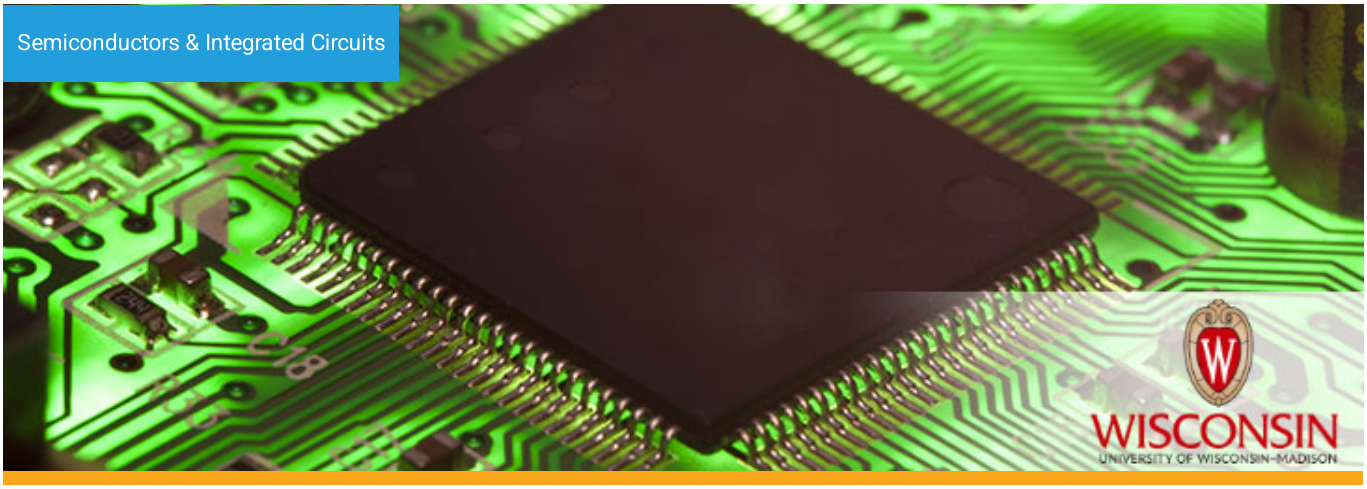


# Thin-Film Semiconductor for Increasing Microprocessor Speeds

View U.S. Patent No. 8,803,195 in PDF format.

**WARF: P07485US**

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**The Wisconsin Alumni Research Foundation (WARF) is seeking commercial partners interested in developing a new process for fabricating heterogeneous semiconductors for improved operational speeds of microelectronics.**

## Overview

Complementary metal-oxide semiconductor (CMOS) technology is commonly used in integrated circuits for microelectronics. Current is produced in semiconductor devices by using mobile charge carriers, either electrons (n-type semiconductor) or holes (p-type semiconductor). The operational speeds of microelectronics are dependent on the electron and hole mobility, with greater mobility leading to faster speed.

Silicon is the primary material used in CMOS technology. Typically, the electron and hole mobility will increase when the silicon undergoes tensile strain. It is widely known that introducing tensile strain in Si(001) increases electron mobility, but at the detriment of hole mobility. Si(110) is better suited for high-hole mobility devices, and applying strain further enhances this characteristic. Combining these materials could lead to a CMOS device with enhanced electron and hole mobility.

Tensile strained mixtures of Si(110) and Si(001) materials can be fabricated by conventional processing methods. However, these processing methods produce low quality semiconductors that form dislocations when stress is introduced to the mixture, resulting in more charge scattering and a subsequent reduction in hole mobility. This contributes to the inability to scale to large devices having optimal charge carrier features when using conventional processes. Additionally, current methods lack a means for constructing semiconductor structures on an array of substrates with more suitable properties for particular applications, such as flexible plastics. New methods for improving the high-electron and high-hole mobility characteristics of CMOS devices are needed.

## The Invention

UW-Madison researchers have developed a method for fabricating a heterogeneous semiconductor structure that enhances both electron and hole mobility. This method extends a previous patent (see WARF reference number P06047US) to allow the fabrication of mixed-crystal-orientation silicon that incorporates the hole mobility enhancing strained Si(110) with the high electron mobility of Si(001).

During fabrication, a thin, single-crystal silicon membrane with regularly patterned holes is applied on a silicon substrate with a different composition, orientation or strain state. The holes then are filled by growing up the bottom layer. Alternatively, the bottom silicon semiconductor layer is patterned with regularly spaced holes. Then a second single-crystal membrane with a different composition, orientation or strain state is applied as a layer over the first and fills the holes. When the top is smoothed, islands of the second layer remain, surrounded by the first. The difference in crystalline orientation, semiconductor composition and/or degree of strain between the silicon layers results in one type of silicon experiencing enhanced electron mobility while the other experiences enhanced hole mobility.



## Applications

- High-carrier-mobility CMOS devices, such as microprocessors

## Key Benefits

- Improves the fabrication quality of a heterogeneous nanomembrane-based semiconductor that can be efficiently scaled for manufacturing
- Increases speed and performance of semiconductor devices
- Offers large-area, single-crystal, high-quality strained-silicon semiconductors on a variety of substrates
- Increases CMOS performance on flexible surfaces, semiconductors, piezoelectrics, and ferroelectrics

## Additional Information

**For More Information About the Inventors**

- Max Lagally

**Related Technologies**

- WARF reference number P06047US discusses the fabrication methods that are used to produce the thin silicon membranes used in this technology.

**Tech Fields**

- Information Technology : Hardware
- Semiconductors & Integrated Circuits : Design & fabrication

For current licensing status, please contact Jeanine Burmania at jeanine@warf.org or 608-960-9846