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**Kim**

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(54) **ENERGY-EFFICIENT MULTICORE PROCESSOR ARCHITECTURE FOR PARALLEL PROCESSING**

(71) Applicant: **Wisconsin Alumni Research Foundation**, Madison, WI (US)

(72) Inventor: **Nam-Sung Kim**, Middleton, WI (US)

(73) Assignee: **Wisconsin Alumni Research Foundation**, Madison, WI (US)

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CPC ..... ***G06F 1/324*** (2013.01); ***G06F 1/3296*** (2013.01); *G06F 1/3228* (2013.01); *G06F 1/3243* (2013.01)

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See application file for complete search history.

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*Primary Examiner* — Phil Nguyen
*Assistant Examiner* — Gary Collins
(74) *Attorney, Agent, or Firm* — Boyle Fredrickson, S.C.

(57) **ABSTRACT**

A multicore computer architecture provides for clock dividers on each core, the clock dividers capable of providing rapid changes in the clock frequency of the core. The clock dividers are used to reduce the clock frequency of individual cores spinning while waiting for a synchronization instruction resolution such as a lock variable. Core power demands may be decreased before and after change in dock speed to reduce power bus disruption.

**19 Claims, 3 Drawing Sheets**